# A Resonant Switch for LNA Protection in Watt-Level CMOS Transceivers

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***Abstract*—An integrated resonant switch designed to protect low-noise amplifier (LNA) circuits in CMOS transceivers is reported. The design implements the receive-path portion of a transmit/receive switch protecting 3-V-process transistors from 5 W (22-V peak) transmit signals while simultaneously helping to achieve a good LNA noise figure on receive and low power loss on transmit. Since the approach is to combine an LNA's matching network and switch functions, the design has no traditional insertion loss on receive. The effective loss to the transmitted signal is less than 0.5 dB using moderate quality inductors ($Q > 6$) and 0.1 dB using $Q = 12$ inductors achievable in most RF-aware CMOS silicon-on-insulator foundries at UHF through $S$-band frequencies.**

***Index Terms*—CMOS transceivers, low-noise amplifier (LNA), transmit/receive (T/R) switch.**

## I. Introduction

RF transceiver implementations have historically relied on a mixed integrated-circuit (IC) approach, with low-noise amplifier (LNA) and power-amplifier (PA) functions in GaAs, up/down-converters in bipolar/BiCMOS, and digital signal processing (DSP) functions in CMOS processes. However, significant strides have been made in implementing full-CMOS designs including LNA and PA circuits on the same die. Recent research on PA design has shown that multiwatt outputs are feasible in standard CMOS with good efficiency [1]. As higher powers are reached, it becomes critical to protect the sensitive gate input of the transceiver's LNA from the high voltages associated with these multiwatt outputs. At a power of only 2 W found in typical time-divsion multiple-access (TDMA) phones, peak voltages on a 50-$\Omega$ antenna reach 14 V. Such voltages will destroy the LNA input transistors if they are not protected in some way. Even for lower power applications, some form of switching is needed to prevent transmit power from being absorbed in the receiver input path.

This paper describes a solution developed during the design of an $L$-band phased-array radar employing a 5-W single-chip silicon-on-insulator (SOI) CMOS transceiver at each antenna.

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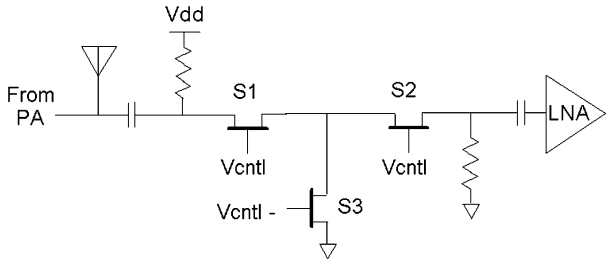


Fig. 1. Typical GaAs T/R switch (after [2]).

The goal is to eliminate the off-chip switch/circulator components traditionally used while maintaining overall system-level performance.

## II. Background

The classic approach to transmit/receive (T/R) switch design, typically implemented in GaAs processes, involves reflective architectures such as that shown in Fig. 1 [2].

If this switch is used between the antenna and LNA, $V\mathrm{cntl}$ is set to a negative voltage and $V\mathrm{cntl}-$ is set to 0 V on transmit, turning off the depletion-mode GaAs MESFETs $S1$, $S2$ and turning on $S3$. $S1$ then presents a high impedance (limited by capacitive parasitics) to the transmit signal. $S3$ shorts any feedthrough to ground while $S2$ provides further isolation if needed. On receive, the control voltages are reversed and $S1, S2$ transfer the signal to the LNA, limited by series resistance in the switches, which degrades the noise figure (NF) to some degree. Reported insertion loss for this design is 1.7 dB, although it is possible to reduce this number through use of larger field-effect transistor (FET) devices and newer processes. Unfortunately, as the FETs are increased in size, parasitic capacitance becomes more pronounced—a problem that has been addressed through various resonant-circuit techniques. One such technique involves resonating the drain–source parasitic capacitances $C_{\mathrm{ds}}$ of FETs such as $S1, S2$ in Fig. 1 with an on-chip inductor [3].

An equally important problem, with or without this isolation-improving technique, is the exposure of switch FET $S1$ to the full voltage at the antenna terminal during transmit mode. With suitable GaAs MESFETs, it is feasible to build switches such as these to handle watt-level signal swings, but in CMOS, breakdown voltages are in the 4-V or below range and these designs become difficult to implement. Recently reported low-loss designs have 1-dB compression points limited to 20–30 dBm

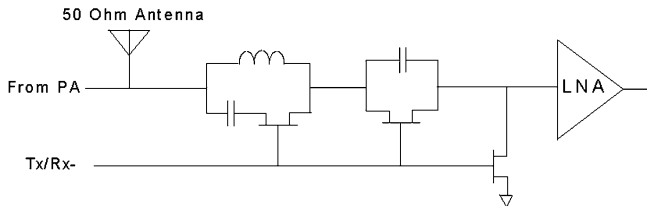


Fig. 2. Monolithic-microwave integrated-circuit (MMIC) resonant switch employing low-voltage shunt transistors (after [6] and [7]).

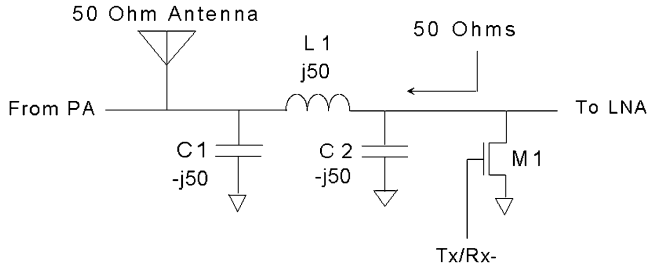


Fig. 3. Receive path design of Talwalkar *et al.* [8] employing shunt switching for LNA protection.

[4].[1] A better approach for high power operation is to employ resonant circuit techniques [5].

Implementations in GaAs have been studied by Tokumitsu *et al.* [6], [7]. As shown in Fig. 2, the LNA is protected by the high impedance of a parallel-tank circuit during transmit. Unlike the previous designs, the switching transistors are *on* during this mode and, hence, have only low voltages across their drain–source. Reported performance with these techniques is a receive insertion loss of 2 dB and transmitter-to-receiver isolation of 30–40 dB while supporting transmit power levels on the order of 30 dBm or above.

More recently, Talwalkar *et al.* [8] have shown a T/R switch employing resonant circuit techniques in CMOS with 1.6-dB insertion loss to the receive path, and 1.6-dB insertion loss to the transmit path while tolerating signal levels of close to 1 W. Their receive path design employs a pi structure, shown in Fig. 3, with a shunt switch $M1$ to protect the LNA on receive. With $M1$ on, $C2$ is shorted to ground and $C1, L1$ form a resonant circuit to create a high impedance (reflective load) to the transmit signal. Thus, the PA output is routed to the antenna. When $M1$ is turned off to place the switch in receive mode, the pi network acts as two $50:25\text{-}\Omega$ $L$-matches back-to-back and simply passes the signal to the LNA with a moderate loss due to the inductor.

While the authors do not explicitly acknowledge it, this shunt-switch technique, with suitable modifications and rethinking, has the potential to achieve the goal of this paper—combining the switch function with a matching network function to decrease loss on both transmit and receive.

## III. Combining Matching and Switching Functions

All the designs in Section II present an insertion loss on receive. Since the switch resides between the antenna and LNA,

[1]Commercial device datasheet. [Online]. Available: http://www.peregrine-semi.com/pdf/pe4259ds.pdf

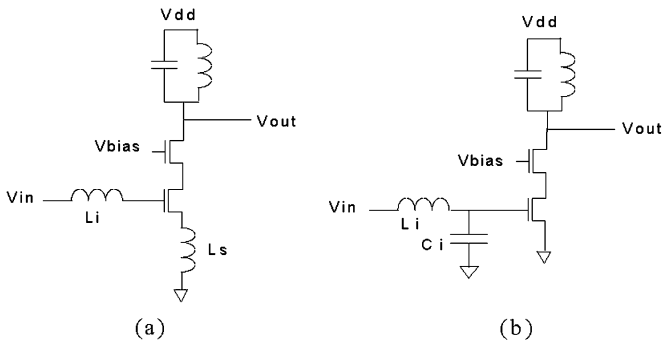


Fig. 4. CMOS LNA topologies: (a) with and (b) without inductive source degeneration.

with 50-Ω terminations assumed on each side, a 1–2-dB insertion loss will degrade the LNA's own NF by 1–2 dB, leading to overall NF values of 3–5 dB or higher for fully integrated designs without the benefit of high-$Q$ off-chip inductors. The solution, as previously stated, is to combine the switching and impedance-matching functions. This technique is especially appropriate for low-interference environments such as the radar transceiver circuits in which the design is being employed. Other potential applications include active RF identification (RFID) tags and low-power wireless sensor networks. Unlike cellular applications where 50-Ω terminations are typically employed to satisfy preselect filter impedance requirements, such systems do not demand a 50-Ω environment past the antenna port.[2]

Two typical LNA designs that achieve good NF at low-to-moderate power consumption are shown in Fig. 4. Both designs improve the NF by using series resonances to provide voltage step-up from the antenna to the LNA transconductor input. In Fig. 4(a), this is achieved while simultaneously providing a resistive input impedance at the operating frequency [9].

An analysis of this design shows that the input impedance is (to first order) [9]

$$Z_{\text{in}} = s\left(L_s + L_i\right) + \frac{1}{sC_{\text{gs}}} + \left(\frac{g_m}{C_{\text{gs}}}\right) L_s \approx \omega_T L_s \quad (1)$$

where $C_{\text{gs}}$ is the FET's input capacitance, $g_m$ is its transconductance, and $\omega_T$ is its current gain-bandwidth product. At the same time, the net transconductance $G_m$ from $V_{\text{in}}$ to drain current is, by virtue of series resonance between $C_{\text{gs}}$ and $L_s + L_i$ [9],

$$G_m = g_m Q_{\text{in}} = \frac{\omega_T}{\omega_o} \frac{1}{2R_s} \quad (2)$$

where $\omega_o$ is the resonant/operating frequency and $R_s$ is the source resistance seen to the left-hand side of the $V_{\text{in}}$ terminal (typically 50 Ω). Note that very large effective transconductances are possible if $\omega_o \ll \omega_T$. This feature, which results from the series-resonant-circuit voltage step-up, is directly responsible for the low NFs possible with this architecture. With the net $G_m$ much larger than the $g_m$ in the FET, the source noise

[2]The other argument often made for 50-Ω termination is for systems where the antenna is remote from the T/R module—a constraint which is not present in the target applications.

contribution to total output noise current in the drain is dominant. An analysis with losses in $L_i$ included shows that the noise factor $F$ is given by

$$F = 1 + \frac{R_i}{R_s} + \gamma g_{do} R_s \left(\frac{\omega_o}{\omega_T}\right)^2 \tag{3}$$

where $R_i$ represents losses in the inductor $L_i$ in the form of an equivalent series resistance and $\gamma g_{do}$ is the product of the FET's channel excess noise factor $\gamma$ and its zero drain–voltage conductance $g_{do}$ [9]. Note that excellent NFs are possible provided the operating frequency is sufficiently below $\omega_T$ and that the series resistance of the input inductor is sufficiently below the antenna source resistance $R_s$. If necessary, $L_i$ can be placed off-chip to achieve the best possible noise performance, and to allow absorption of bond-wire parasitics if a low-inductance package is not available.

In Fig. 4(b), the voltage step-up is provided without resistive impedance formation. This design presents a short circuit (ideally) at the amplifier input, but still produces good gain and NF due to the series resonance. The performance can be found from (1)–(3) with $L_s$ set to zero and with $C_{\rm gs}$ replaced with $C_{\rm gs}+C_i$ and $\omega_T$ replaced by

$$\omega_T' = \omega_T \left(\frac{C_{\rm gs}}{C_{\rm gs}+C_i}\right). \tag{4}$$

Clearly $C_i$ should be minimized for good NF, producing a high-$Q$ resonance and a high impedance seen looking back through the $L$-match toward the source. The practical limitation comes from parasitic capacitances, as well as the maximum value, which $L_i$ can reach before $R_{\rm in}$ in (3) becomes too large.

The design of Fig. 4(b) is permissible in applications such as radar and satellite receivers, which mount the LNA immediately at the antenna and which, by virtue of antenna pointing selectivity and half-duplex operation, do not require additional preselect/duplex filtering beyond that provided by the antenna and matching network. This is viable as well in applications where a suitably designed integrated LNA provides some inherent preselection itself [10], [11].

It is also possible to combine the two approaches, placing a source inductor into the Fig. 4(b) circuit and absorbing the residual capacitive component of the input impedance into the matching network $L_i, C_i$. This latter approach is used in a transceiver circuit example discussed in Sections VII and VIII.

## IV. Proposed Switch Design

The proposed receive switch design for either of these circuits is shown in Fig. 5. For simplicity, the LNA topology of Fig. 4(b) is assumed.

During receive, both switches are open and $L1, C2$ form an $L$-type impedance step-up network to increase the antenna voltage seen by the LNA and, hence, reduce NF as previously elaborated in (2) and (3). Note that FET $M2$ is in parallel with both $C2$ and the input capacitance of the cascode LNA so that their parasitic capacitances can be absorbed as needed. If $L1$ is placed off-chip to maximize its $Q$ and minimize its NF, $C2$ can also absorb pad capacitance parasitics.

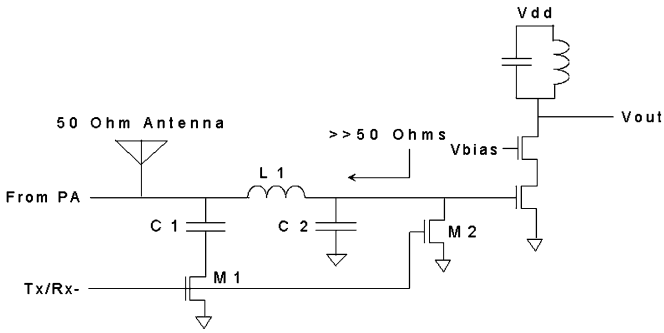


Fig. 5. Proposed switch connected to representative LNA circuit (optional source inductor not shown).

On transmit, both switches are closed and $L1, C1$ form a parallel-resonant circuit to minimize loading on the transmitter feeding the antenna. Letting $X_{L1}$ be the reactance of $L1$ at resonance, and $Q$ be its quality factor, the transmit-mode input impedance $R_{\rm in\_tx}$ is simply

$$R_{\rm in\_tx} = QX_{L1}. \tag{5}$$

This value is much greater than 50 $\Omega$ since $Q \gg 1$ and $X_{L1} > 50$ for good NF. For example, assuming a moderate impedance step-up between 4 and 16 in the matching network, component reactances will range from 100 to 200 $\Omega$ and the loading on the transmitter will be 500–2 k$\Omega$ with a moderate $Q$ (5–10) inductor realization. This large resistance relative to a 50-$\Omega$ antenna impedance will not significantly change the load resistance seen by the transmitter so that little load pulling will result. Moreover, the power absorbed by the network relative to the transmitter output power will be small. Letting $V_{\rm ant}$ be the antenna voltage during transmit, and $R_{\rm ant}$ be its impedance alone, this ratio is

$$\frac{P_{\rm absorbed}}{P_{\rm tx}} = \frac{V_{\rm ant}^2/R_{\rm in\_tx}}{V_{\rm ant}^2/\left(R_{\rm ant}||R_{\rm in\_tx}\right)} = \frac{R_{\rm ant}||R_{\rm in\_tx}}{R_{\rm in\_tx}}. \tag{6}$$

Evaluating (6) for the case above results in an absorption of 9%–2.4% of the transmit power, translating to an effective loss of only 0.4–0.1 dB respectively.

In addition to $L1, C1$ forming a reflective termination as seen by the transmit signal, $L1, M2$ form an attenuator to decrease the voltage seen by the LNA. At the same time, the relatively high reactance of $L1$ limits ac currents to reasonable levels so that metal width in the inductor and associated circuits are kept to manageable dimensions.

Comparing the design of Fig. 5 with that of Fig. 3, the new technique integrates an $L$-type step-up matching network with the switching function to obtain good overall NF rather than acting as a standalone switch with associated additional losses. The only significant negative effects are the noise contributed by the matching inductor itself, which is needed in any case. Moreover, the inductor $L1$ in the $L$-match will typically have a higher reactance $X_L$ than the separate-switch pi topology. Hence, the inductor currents $(V_{\rm ant}/X_L)$ in transmit mode are less, allowing higher transmit power to be tolerated. In addition, power loss in transmit mode (inversely proportional to $Q$ times $X_L$) is less for a given inductor $Q$. Finally, the design offers increased degrees

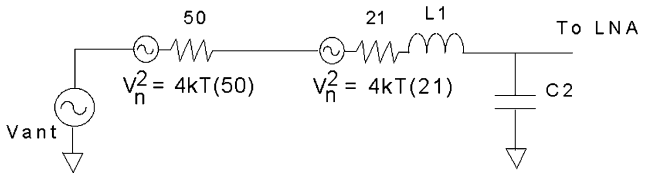


Fig. 6. Approximate noise model of $L$-match.

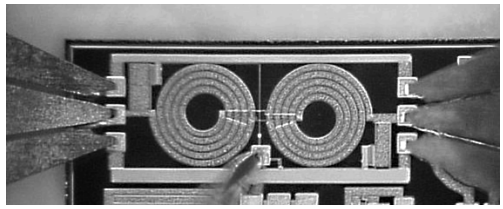

Fig. 7. Die photograph of prototype switch.

of freedom in achieving the resonance between $L1, C1$ since the value of $C1$ is not a significant factor on receive.

## V. Prototype Implementation

To validate the approach, a representative prototype switch was designed and fabricated in a 0.35-$\mu$m CMOS SOI process with moderate $Q$ inductors. The prototype matches the schematic of Fig. 5 minus the LNA and was designed for a nominal operating frequency of 1.2 GHz using $C1 = 0.9$ pF, $C2 = 0.65$ pF, and $L1 = 16.4$ nH (two 8.2-nH spirals in series, each with a measured $Q$ of 6). $C2$ is smaller than $C1$, as discussed earlier, to absorb parasitic drain–source capacitance of $M2$, which has $W/L = 400/0.35$, a $C_{\rm ds}$ value of approximately 0.2 pF, and a designed $R_{\rm on}$ value of 5 $\Omega$. Both are slightly smaller than the calculated resonating value due to compensation for capacitive parasitics from the spiral inductors.

With these component parameters, the expected $Q$ of the *LC* tank in transmit mode is $125/(21 + 5 + 4) = 4.2$ and the impedance in parallel with the antenna is 500 $\Omega$—corresponding to 10% power absorption or 0.5 dB loss. The predicted attenuation of the transmit antenna voltage to the LNA input is 0.04, allowing signals in excess of 5 W to be tolerated without exceeding 1-V peak at the LNA. At the same time, the moderately high 125 $\Omega$ reactance of $L1$ keeps ac current density within a typical 3-mA/$\mu$m top-metal ac electromigration limit for the 60-$\mu$m inductor trace width used.

In receive mode, the series-resonant tank formed by $L1, C2$ is 21 $\Omega$ (assuming negligible loss in $M1, M2$ when off), resulting in a loaded $Q$ of $125/(21 + 50) = 1.8$, an impedance step-up from 50 to 300 $\Omega$, and a voltage step-up ratio of 2 from the open-circuit antenna voltage (4$\times$ relative to the 50-$\Omega$ loaded antenna voltage). As previously discussed, this voltage amplification is critical to obtaining good NF in an attached LNA intended for low power consumption. However, one must also consider the losses within the inductor itself and its effect on the NF, as shown in Fig. 6.

With the moderate $Q$ inductors used, the source noise is increased by 71/50, which translates to an NF hit of 1.5 dB. While this value is significant, it should be noted that it is due to the integrated LNA input impedance match rather than the switch and would be increased further by the approximate 2-dB insertion if the earlier switch designs were used. While it is true that a pi network such as that used in Fig. 3 can also perform impedance transformations, the requirement to present a specific resonant frequency on transmit constrains this. In addition, the pi match will necessarily have higher losses due to its operation as two back-to-back $L$-matches. The circuit of Fig. 5 is intentionally designed to combine matching with switching using a lower-loss $L$-network and can implement the required resonance frequency on transmit over a wide range of impedance transformations. It should also be noted that higher $Q$ inductors (e.g., $Q = 12$) possible with thicker metal and/or higher frequency operation could decrease the NF hit to 0.8 dB or less in the new architecture—providing the possibility of a combined switch/LNA fully integrated in CMOS with very low *overall* NF.

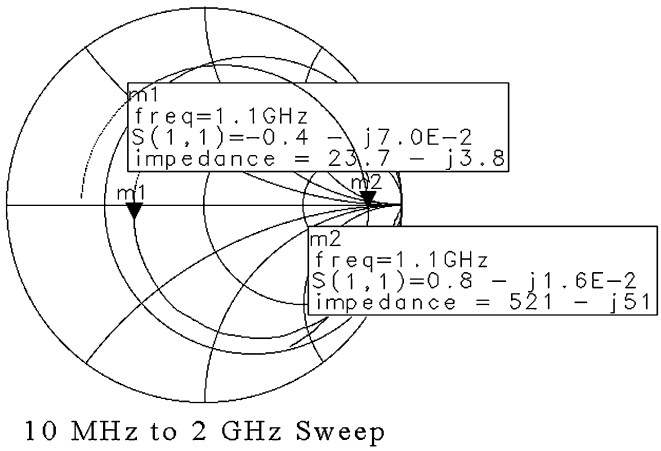


Fig. 8. $S11$ values of Fig. 7 circuit at input (antenna port) in transmit and receive mode with output (LNA port) open (calculated from measured two-port $S$-parameters).

## VI. Measured Results

A fabricated prototype is shown in Fig. 7 undergoing two-port network analyzer measurements with ground–signal–ground (GSG) probes. Measured $S11$ (at the antenna port end with LNA port open) is shown in Fig. 8 for the case of both receive and transmit modes. In both cases, the resonant frequency was found to be 1.1 GHz, indicating the design target of 1.2 GHz was missed by approximately 10% and minor adjustments are needed to achieve design centering in the next revision. In receive mode, the series-resonant input impedance at the actual resonant frequency of 1.1 GHz is 23.7 $\Omega$ (suggesting some small additional losses from the off-state switches) and, in transmit mode, the parallel-resonant impedance is 521 $\Omega$. Both of these are close to the predicted values, validating that NF and PA efficiency hits of 10% and $<$2 dB are obtainable, even with $Q = 6$ inductors.

Transmission values derived from measurements in receive and transmit modes are shown in Fig. 9 and are also close to predicted values. As in the reflection measurement case, these are plotted for the case where the LNA port is modeled as a capacitive input impedance whose $C$ is absorbed into $C2$. During receive, the matching network provides a boost of 1.7$\times$ relative to

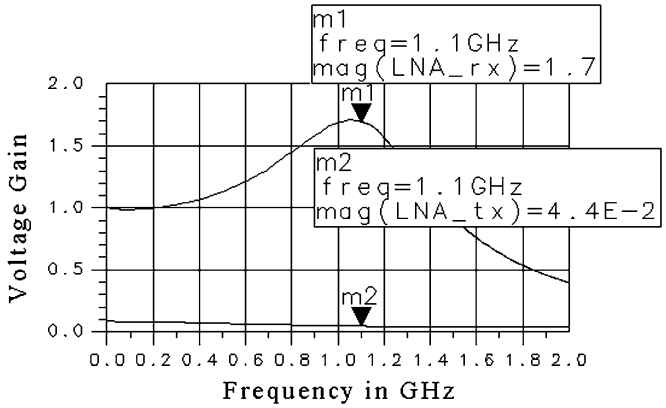


Fig. 9. Voltage gain from antenna port to LNA port in transmit and receive with LNA port open (calculated from measured two-port $S$-parameters).

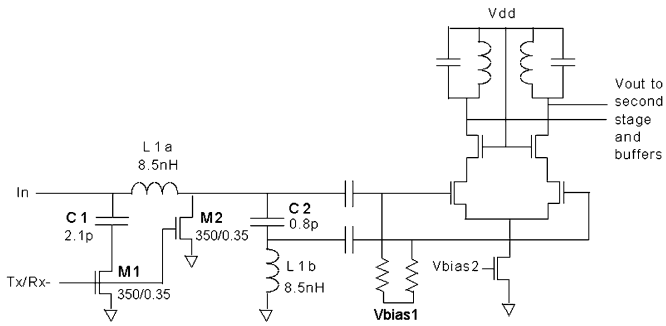


Fig. 10. Simplified schematic of differential LNA incorporating switch/matching-network/balun circuit.

the received open-circuit antenna voltage at 1.1 GHz (3.4× relative to a 50-Ω loaded value). In transmit mode, the RF voltage on the antenna is reduced by 0.044, which corresponds to reduction of a 5-W (22-V peak) signal to an easily tolerated 1-V peak at the LNA port.

## VII. Application Circuit Examples

The switch concept described is currently being designed into two systems—an $L$-band phased-array radar with a separate T/R module at each antenna, and a very low power UHF transceiver IC. In the case of the radar, low power is required due to the multiplication of the LNA power by thousands of array elements. A simplified schematic of the LNA together with the switch is shown in Fig. 10. In this circuit, the switch/matching network also doubles as a balun to convert the signal to differential form on receive. Hence, the implementation is more elaborate than that of Fig. 5.

A die photograph of the circuit is shown in Fig. 11, and the measured $S11$ and $S21$ on transmit and receive are shown in Fig. 12. Note that the overall behavior matches the previously discussed behavior, except that the transmit-mode input impedance is only 200 Ω and the transmit signal is reduced by only 0.1 (as seen by the −20-dB step in measured $S21$ when switched from the receive to transmit mode). This is due to a design decision to implement a balun function and place $M2$ at the center of the two inductors. In the next revision, the circuit of Fig. 5 will be used directly and the LNA input stage will

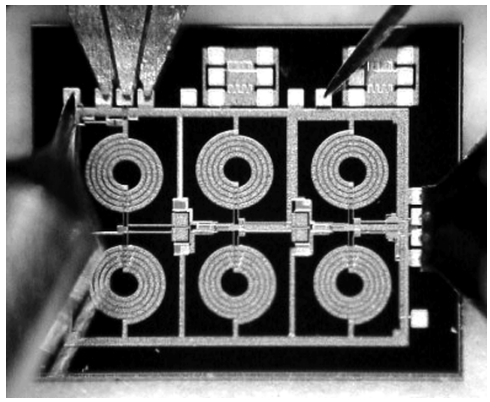

Fig. 11. Die photograph of LNA.

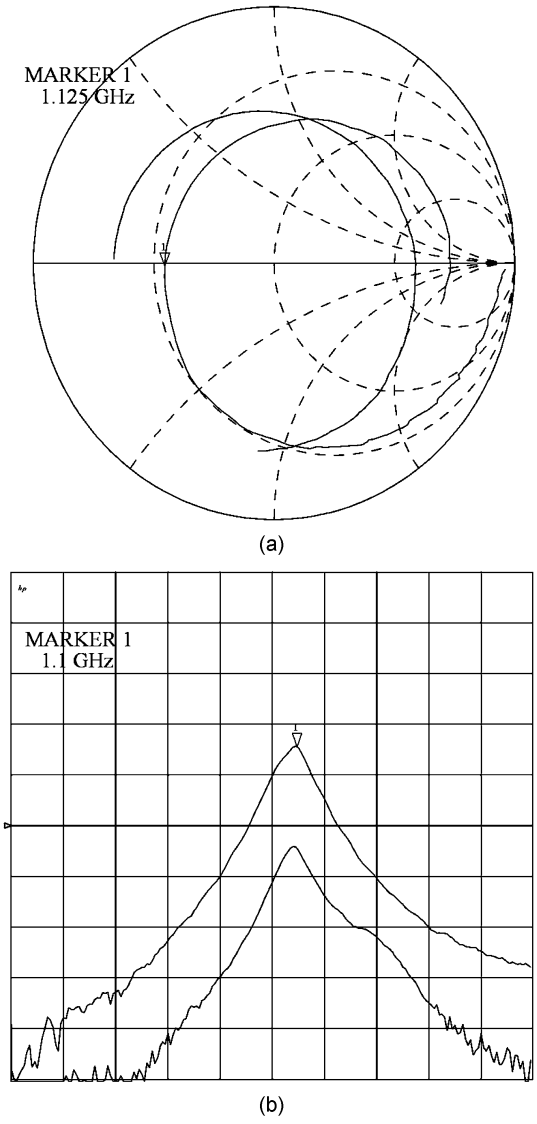


Fig. 12. Measured: (a) $S11$ and (b) $S21$ from 10 MHz to 2 GHz on transmit and receive. Vertical scale is 10 dB/div in $S21$ plot.

perform the balun operation by ac terminating the opposite input so that a higher $Z$ and attenuation will be present during transmit. Simulation indicates that the performance of the basic switch in Figs. 8 and 9 can be reached with this modification.

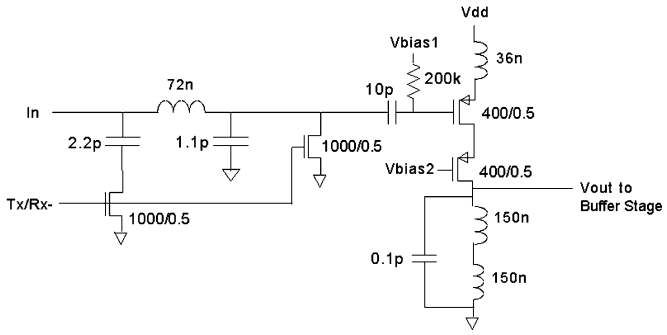


Fig. 13. Single-ended UHF LNA using integrated switch/matching-network.

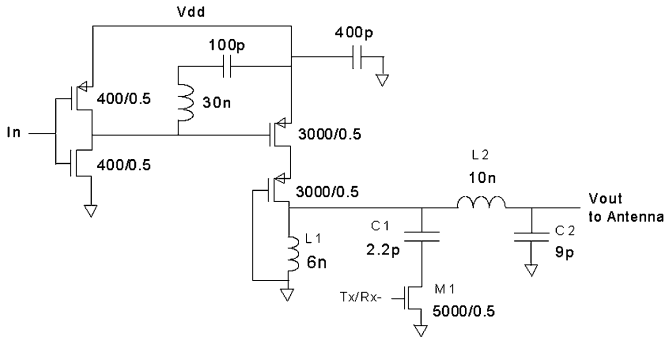


Fig. 14. Simplified schematic of 400-MHz PA.

Measured NF of the amplifier was approximately 3.5 dB at 8-mA current draw (excluding 50-$\Omega$ output buffers). While slightly above target, this result includes the fully integrated switch function and is adequate for the intended application.

A lower NF LNA design incorporating the switch technology is shown in Fig. 13. This LNA is designed for use in a UHF microtransceiver using silicon-on-sapphire (SOS). It operates at 430 MHz while drawing less than 1 mA from a 3-V supply.

Simulated power gain is 17 dB and the simulated NF is 2.7 dB using $Q = 10$ inductors. In transmit mode, the simulated input-port impedance is 1200 $\Omega$, absorbing only 4% (0.2 dB) from the transmit signal power. Note that p-channel FETs are used due to their lower (nearly ideal) measured gamma factor in the target process [11]. Note also that the inductor values are large due to operation at UHF, as well as the need to achieve good NF with only 1-mA current consumption. Such inductors are possible with $Q$ up to ten in SOS by taking advantage of the insulating substrate, 3-5-$\mu$m metal, and large physical dimensions (600 $\mu$m for the input inductor) [11].

## VIII. Transmitter Switch Considerations

To implement a fully integrated transceiver, a transmit-side switch is required in addition to the receive switch discussed in this paper. One alternative is to use a pass transistor and substrate *LC*-tuned substrate bias [8] and accept the 1.5 dB of insertion loss. Another is to employ the concept of integrating matching networks with the switching function, as done with the LNA.

To achieve moderate-to-high power in a CMOS PA, either a matching network is required to transform the 50-$\Omega$ antenna load to a lower value, and/or some form of transformer combining is required. An example class-D cascode 150-mW PA using the former technique alone is shown in Fig. 14.

This 400-MHz PA is designed as a companion to the LNA of Fig. 13. On transmit, $M1$ is on, switching in capacitance to resonate with $L1$ (together with transistor parasitics). Since $M1$ is on, the voltage across it is limited to very low values, providing low loss, good linearity, and no breakdown concerns. Simulated efficiency of the PA under this condition is approximately 40%. When placed in receive mode, $M1$ is turned off and $L1, L2$ achieve a total of approximately 16 nH (excluding parasitic effects) to resonate with $C2$ at the 430-MHz receive frequency. The simulated impedance seen looking back into the PA from the antenna port is shown in Fig. 15.

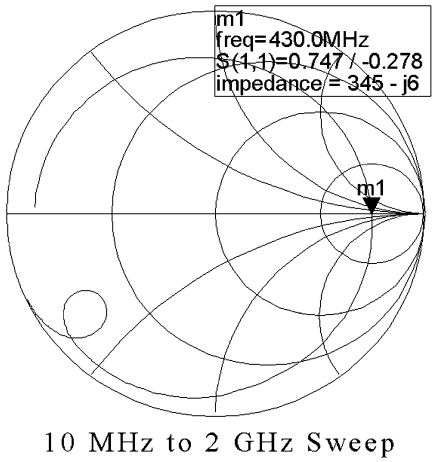


Fig. 15. Simulated $S22$ of PA in receive mode using $Q = 12$ inductors.

At the receive frequency, this impedance (using $Q = 10$ inductors) is 350 $\Omega$, which implies a small amount of attenuation to the receive signal and a small amount of additional noise. Extending the circuit of Fig. 13 to include these effects shows a total 3.5-dB NF. Comparing this to the 2.7-dB value previously found with the LNA/switch alone implies a modest 0.8-dB additional degradation when the transmitter is connected to the antenna. In a total transceiver link budget, this NF hit must be traded against the potentially higher transmit efficiency hit of a more traditional switch design. For example, in the radar application envisioned, NF and PA efficiency can be traded directly and this PA switch technique becomes competitive.

## IX. Conclusion

Significant strides are being made in integrating moderate to high-power PA designs into low-voltage CMOS processes. To allow such designs to be integrated on the same die as the LNA and other RF circuits, the LNA must be isolated, as well as protected from the large RF voltage swings present at the antenna port. Traditional reflective switches are unsuitable since deep submicrometer CMOS processes have breakdown voltages of 4 V or less. The solution is to use shunt switches, which are in the on-state during transmit, together with resonant circuits to combat parasitic capacitance limitations. In this paper, these techniques are employed while simultaneously integrating matching networks with the T/R switch function. The resulting LNA-protection circuit enables full integration while achieving

good performance (0.5-dB effective transmitter power loss and approximately 2.5–3.5-dB total NF) with only moderate quality ($Q = 6$–$10$) inductors at UHF through $L$-band. Designs implemented with better inductors (e.g., $Q = 12$ to $20+$), which are possible at higher frequencies of operation in SOI processes with very high-resistivity substrates, could potentially improve these values to $<0.2$ and $<2$ dB, respectively.

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